

What is claimed is:

1. A method, comprising:

2. The method of claim 1, further comprising:

3. The method of claim 1, further comprising:

4. An apparatus, comprising

an arbiter linked to a first processor having a flexible architecture;

a point to point bus; and

a device, the first processor connected to the device through the point to point bus.

5. The apparatus of claim 4, wherein the arbiter is internal to the first processor.

6. The apparatus of claim 4, wherein the arbiter is external to the first processor.

7. The apparatus of claim 4, wherein the arbiter comprises a component to change a number of ports linked between the first processor and the device without changing the flexible architecture within the processor.

8. The apparatus of claim 4, wherein the device is selected from the group consisting of an input-output component, a bridge, a chipset, a memory, or a second processor.

9. The apparatus of claim 4, wherein the processor comprises:

a protocol layer;

an information transfer layer to electronically transfer information on a physical medium between the protocol layer and the device; and

a buffer layer to buffer an electronic transfer of information between the protocol layer and the information transfer layer.

10. The apparatus of claim 4, wherein the arbiter comprises a first component and a second component, the first component to determine a bandwidth between the device and the processor, the second component to provide a control signal to one or more signal pathway switching devices, the control signal to be based upon the bandwidth determination of the first component.

